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Attorney Docket No.: PA000419
Date: 29 September 2000
Express Mail Label No.: EL055395957US

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Transmitted herewith for filing is the patent application of:
Inventor(s):   Sindhushayana, et al.
For: Method and Apparatus for Reducing Power Consumption of a Decoder in a Communication System

Enclosed are:
1. ☒ Patent application (19) total pages.
2. ☒ Drawings: ☐ Formal (   ) sheet(s) or ☒ Informal (2) sheet(s).
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4. ☐ An Assignment (   ) pages and Recordation Form Cover Sheet.
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Multiple Dependent Claim(s): ☐ No ☐ Yes			$260	$
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Date: 29 September 2000

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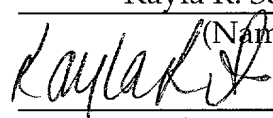|	
In Re Application of	)
	) For: Method and Apparatus for Reducing
Sindhushayana, et al.	) Power Consumption of a Decoder in a
	) Communication System
Serial No. Unknown	)
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METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION OF A DECODER IN A COMMUNICATION SYSTEM

5   ## BACKGROUND OF THE INVENTION

I. Field of the Invention

The current invention relates to communications. More particularly, the present invention relates to a novel method and apparatus for reducing power 10 consumption of a decoder in a communication system.

II. Description of the Related Art

Several communication systems exchange data organized into packets, 15 among the terminals in a communication system. For the purposes of this description, a packet is a group of bits, including data (payload) and control elements, arranged into a specific format. The packets to be communicated are formatted in accordance with a selected communication channel structure. In general, a communication channel structure is comprised from smallest 20 organizational structures, e.g., slots. For the purposes of this description, a slot is a fixed time interval comprising a variable number of bits depending on a data rate. When the number of bits of a packet exceeds the number of bits in a slot, the packet must be communicated over several slots as a multi-slot packet. The packet may be arranged among the slots of the communication channel 25 structure so that each slot following the first slot contains redundant bits of the packet with respect to the first slot. Consequently, the whole payload content of a currently sent packet has been communicated to a receiving station when the first slot has been communicated. Therefore, if the receiving station can decode the current packet before it has been transmitted in its entirety, it can 30 notify a transmitting station, and the transmission of the current packet can be terminated, thereby increasing the effective data rate.

The straightforward method of determining whether a current packet can be decoded early is to attempt decoding after each slot of the multi-slot transmission. However, this strategy results in high power consumption by the 35 decoder.

Consequently, there is a need for a strategy aimed at minimizing decoder power consumption, while providing the benefits of early termination.

SUMMARY OF THE INVENTION

The present invention is directed to a novel method and apparatus for a method for reducing power consumption of a decoder in a communication system. Accordingly, in one aspect of the invention a quality metric of a segment of a received signal is estimated. Then a quality metric threshold is determined and an interval in accordance with a modified quality metric threshold is delimited. If the estimated quality metric is outside of the interval, the segment is decoded.

In another aspect, the decoding process comprises delimiting a plurality of intervals in accordance with the quality metric threshold, associating each of the plurality of intervals with one of a plurality of parameters, determining an interval from the plurality of intervals into which the estimated quality metric belongs; and decoding the received signal for a number of iterations equal to the one of a plurality of parameters associated with the determined interval.

In another aspect, a stopping criterion is evaluated in the course of the decoding process, and the decoding process is terminated in accordance with the stopping criterion.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objectives, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify elements correspondingly throughout and wherein:

FIG. 1 illustrates an exemplary communication system capable of implementing embodiments of the invention;

FIG. 2 illustrates a flow chart of a decoding process in accordance with one embodiment;

FIG. 3 illustrates a conceptual forward link structure in accordance with one embodiment of the invention;

FIG. 4 illustrates a conceptual forward link structure in accordance with another embodiment of the invention.

FIG. 5 illustrates a block diagram of an apparatus in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Overview

FIG. 1 illustrates an exemplary communication system **100** capable of implementing embodiments of the invention. A transmitting station (TS) **102** transmits signals to a receiving station (RS) **104** over a forward link **106a**. Because the signals transmitted from the TS **102** contain user data, the forward

5 link must comprise at least a traffic channel. The TS **102** receives signals from the RS **104** over a reverse link **106b**. Because the signals transmitted from the RS **102** do not need to contain user data, the reverse link need not comprise a traffic channel. If a two-way user data communication is desired, both the forward link **106a** and the reverse link **106b** must comprise traffic channels. For

10 simplicity, the communication system **100** is shown to include only two stations. Such a system can represent, e.g., two computers communicating with each other. However, other variations and configurations of the communication system **100** are possible. In a multi-user, multiple-access communication system, single TS may be used to concurrently or sequentially

15 transmit data to and receive data from a number of RSs.

There are several multi-user, multiple-access communication systems, utilizing techniques such as: time division multiple-access (TDMA), frequency division multiple-access (FDMA), amplitude modulation (AM) schemes, and other techniques known in the art. Another type of multi-user, multiple-access

20 communication system technique is a code division multiple-access (CDMA) spread spectrum system that conforms to the "TIA/EIA/IS-95 Mobile Station-Base Station Compatibility Standard for Dual-Mode Wide-Band Spread Spectrum Cellular System," hereinafter referred to as the IS-95 standard. The use of CDMA techniques in a multiple-access communication system is

25 disclosed in U.S. Patent No. 4,901,307, entitled "SPREAD SPECTRUM MULTIPLE-ACCESS COMMUNICATION SYSTEM USING SATELLITE OR TERRESTRIAL REPEATERS," and U.S. Patent No. 5,103,459, entitled "SYSTEM AND METHOD FOR GENERATING WAVEFORMS IN A CDMA CELLULAR TELEPHONE SYSTEM," both assigned to the assignee of the present invention

30 and incorporated herein by reference.

The communication system **100** may carry voice and/or data. Examples comprise communication systems conforms to the "3rd Generation Partnership Project" (3GPP) and embodied in a set of documents including Document Nos. 3G TS 25.211, 3G TS 25.212, 3G TS 25.213, and 3G TS 25.214 (the W-CDMA

35 standard), or "TR-45.5 Physical Layer Standard for cdma2000 Spread Spectrum Systems" (the IS-2000 standard). Another example of a communication system carrying both voice and data is a system in accordance with the IS-95 standard, which specifies transmitting traffic data and voice data over the forward and reverse links. A method for transmitting traffic data in code channel frames of

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fixed size is described in detail in U.S. Patent No. 5,504,773, entitled "METHOD AND APPARATUS FOR THE FORMATTING OF DATA FOR TRANSMISSION", assigned to the assignee of the present invention and incorporated by reference herein. In accordance with the IS-95 standard, the

5   traffic data or voice data is partitioned into code channel frames that are 20 milliseconds wide with data rates as high as 14.4 Kbps.

An example of a data only system is a high data rate (HDR) system, such as a system disclosed in co-pending application serial number 08/963,386, entitled "METHOD AND APPARATUS FOR HIGH RATE PACKET DATA

10   TRANSMISSION," filed 11/3/1997, assigned to the assignee of the present invention and incorporated by reference herein.

The forward link **106a** and the reverse link **106b** can propagate through a guiding media, e.g., a wire, a coaxial cable, an optical cable or other media known to one skilled in the art, or in case of wireless link through free space.

15   The communication system **100** may employ variable data rate transmission on the forward link **106a**. Such a system, disclosed in co-pending application serial number 08/963,386, defines a set of data rates, ranging from 38.4 kbps to 2.4 Mbps, at which an access point (e.g., TS **102**) may send data packets to an access terminal (e.g., RS 104). In one embodiment, the data rate is

20   determined by a data rate selection method at the RS **102**, and a scheduler method at the TS **104**. Although the data rate determination is described in terms of the data rate selection method and the scheduler method, one of ordinary skill in the art will understand that this is for illustration only, and any data rate determination method can be used.

25

Data Rate Selection Method

A rate control method enables an RS (e.g., RS **104**) to determine the TS from which the RS **104** can receive the best throughput. The rate control method further enables the RS **104** to estimate the maximum data rate at which

30   the RS **104** can receive the next signal segment from the selected TS.

In one embodiment, each TS in the communication system **100** transmits known signal, called a pilot signal, at well-defined, periodic intervals. The RS **104** monitors the pilot signals received from the TSs in he RS **104** active set, and utilizes the pilot signals to determine a quality metric associated with each TS.

35   In one embodiment, the quality metric is a signal-to-noise ratio (SINR). For the purposes of this description, an active set is a list of pilot signals selected by the particular RS from all pilot signals received with sufficient strength to indicate that the associated forward traffic channel can be successfully demodulated. Based on the SINR information over past signal segments from each of the TSs

in the RS **104** active set, the RS **104** predicts the SINR over future signal segment(s) for each of the TSs in the RS **104** active set. In one embodiment, the signal segment is a slot. An exemplary prediction method is disclosed in co-pending application serial number 09/394,980 entitled "SYSTEM AND METHOD FOR ACCURATELY PREDICTING SIGNAL TO INTERFERENCE AND NOISE RATIO TO IMPROVE COMMUNICATIONS SYSTEM PERFORMANCE," assigned to the assignee of the present invention and incorporated herein by reference. The RS **104** then selects the TS (e.g., TS **102**), which offers the best throughput over the future slot(s), and estimates the highest data rate at which the RS **104** can receive the next packet from the TS **102**. The RS **104** then sends a data rate request (DRC) to the TS **102**, indicating the data rate at which the RS **104** wishes to receive the next packet.

Scheduling Method

A scheduling method enables a TS that received the DRC (e.g., TS **102**) to determine an RS (e.g., RS **104**), to which the TS **102** should transmit the next packet at the data rate requested by the RS **104**. The scheduling method at the TS **102** monitors the sequence of DRCs from all RSs that wish to receive data from the TS **102**. In accordance with the received DRCs, the TS **102** determines the RS to which the TS **102** should send the next packet, in order to maximize the forward link throughput while maintaining acceptable link performance at each RS.

Need for Early Termination

In one embodiment, employing data rate determination in accordance with the described rate control method and scheduler method, the need for early termination arises as follows.

The data rate, requested by the RS **102** via a DRC from the TS **104**, is determined using the rate control method, which predicts a SINR over future slot(s) based on the SINR over past slot(s) from the TS **104**. The SINR from the TS **104** is subject to rapid, unpredictable changes due to the variations in the channel. Such variations include signal-to-noise ratio changes, fading, time variance, and other changes known to one skilled in the art. Because these variations are different for different communication channels, transmission of a signal over a wireless communication channel requires different considerations than transmission of a signal over a wire-like communication channel, e.g., coaxial cable, optical cable, and other types known to one skilled in the art. One of the factors affecting the communication channel characteristics in wireless communication systems is inter-cell interference. Such interference levels may

be significantly higher during the data transmission than the interference level seen during the pilot transmission, because some of the base stations may remain idle during the data period. Consequently, it is not always possible for the RS **104** to predict the SINR with great accuracy. Therefore, the rate control

5 method establishes a lower bound on the actual SINR during the next packet duration with high probability, and determines the maximum data rate that can be sustained if the actual SINR is equal to this lower bound. In other words, the rate control method provides a conservative measure of the rate data at which the next packet can be received.

10 Early termination of current packet transmission attempts to refine this estimate, based on a quality metric of a signal received during the initial slots of the current packet transmission. Based on the channel conditions, or equivalently, the initial uncertainty about the SINR over future slot(s), the RS **104** may decode the current packet before it has been transmitted in its entirety.

15 As discussed, this significantly increases the forward link throughput of the communication system.

Early Termination of Current Packet Transmission

The following embodiment describes an early termination method,

20 which can be used regardless of the method employed to determine a data rate, and the particular factors influencing the need for early termination.

At the end of each slot over which the RS **104** is receiving a current packet at a current data rate, the RS **104** computes a quality metric. In one embodiment, the quality metric is an average SINR. In one embodiment, each

25 TS in the communication system **100** transmits known signal, called a pilot signal, at well-defined, periodic intervals. The RS **104** monitors the pilot signal in the slot over which the current packet was received, and utilizes the pilot signal to compute the average SINR.

For each data rate, the RS **104** maintains a table that maps a number of

30 slots of transmission onto an average SINR required to decode a current packet with a reasonably low error rate. In one embodiment, the entries in this look-up table are based on simulation or controlled tests of RS demodulator performance under various channel conditions. Thus, the look-up table defines required packet SINR (SINR threshold) for a given data rate and for a given

35 number of transmitted slots. Consequently, the average SINR provides an indication of a probability of successful decoding of the current packet at the current data rate, using the data from the slots received so far. One of ordinary skill in the art will further understand that although the early termination

method described below is described in terms of variable data rate, this is for instructive purpose only.

An actual average packet SINR may be higher than the average SINR computed by the RS **104** because the SINR computed by the RS **104** is subjected to measurement noise, thereby inducing some uncertainty in the actual average SINR. In one embodiment, such measurement noise may be induced by interfering TSs. In one embodiment, a decoder carries out a decoding process as a series of iterations. An example of such a decoder is a turbo code decoder, described below. A general early termination method is as follows:

Let $\Delta_0 \leq \Delta_1 \leq ... \leq \Delta_m \leq 0 < \Delta_{m+1} \leq \Delta_{m+2} \leq ... \leq \Delta_{m+n}$, be real-valued parameters, and let $N_1 \leq ... \leq N_m \geq N_{m+1} \geq N_{m+2} \geq ... > N_{m+n+1}$ be non-negative, integer-valued parameters, where m, n are be non-negative, integer-valued parameters. Let AS denote the average packet SINR measured over past transmitted slot(s) of a current packet transmission, and TS denote the SINR threshold for the given data rate, over the past transmitted slot(s). Then:

If $AS < TS + \Delta_0$, do not attempt to decode the current packet with currently available data.

If $TS + \Delta_{k-1} \leq AS < TS + \Delta_k$, attempt to decode the current packet with a maximum of N_k iterations, for all $k \in [1, m+n]$.

If $AS \geq TS + \Delta_{m+n}$, attempt to decode the packet with a maximum of N_{m+n+1} iterations.

The decoding process in accordance with one embodiment is described in reference to **FIG. 2.**

The method starts in step **202** upon receiving a current packet. The method continues in step **204.**

In step **204**, an average SINR (AS) is computed at the end of a particular slot of a current packet transmission. The method then continues in step **206.**

In step **206**, an SINR threshold (TS) for the given data rate over the given number of transmitted slots is determined. The method then continues in step **208.**

In step **208**, a condition $AS < TS + \Delta_0$ is evaluated. In one embodiment, the parameter Δ_0 is determined in accordance with a simulation or controlled test of RS demodulator performance under various channel conditions. If the condition $AS < TS + \Delta_0$ is satisfied, the method continues in step **210**. If the condition $AS < TS + \Delta_0$ is not satisfied, the method continues in step **212.**

In step **210**, the decision not to attempt decoding with currently available data is made because the average SINR computed is considerably lower than the corresponding SINR threshold. Consequently, it is very unlikely that the

packet can be correctly decoded using the data from the slots received so far. The method returns to step **204**.

In step **212**, an auxiliary variable k is set to a value of 1. The method continues in step **214**.

In step **214**, a condition $TS + \Delta_{k-1} \leq AS < TS + \Delta_k$ is evaluated. In one embodiment, the parameters Δ_k, Δ_{k-1} are determined in accordance with simulation or controlled test of RS demodulator performance under various channel conditions. If the condition $TS + \Delta_{k-1} \leq AS < TS + \Delta_k$ is satisfied, average SINR computed is not considerably low, but still well below the SINR threshold. Consequently, the packet may be correctly decoded if the actual SINR over the slot is significantly higher than the SINR measured over the pilot signals. Therefore, the method continues in step **216**. If the condition $TS + \Delta_{k-1} \leq AS < TS + \Delta_k$ is not satisfied, the method continues in step **224**.

In step **216**, a decoding attempt with currently available data is carried out for a first pre-determined number of iterations N_k. The method continues in step **218**. Step **OPT**, representing a dynamic stopping rule, interposed between step **216** and step **218**, is optional. The step **OPT** is described below.

In step **218**, a success of the decoding attempt is ascertained. In one embodiment, the success is ascertained in accordance with the method described below in connection with the dynamic stopping rule. If the decoding is unsuccessful, the method returns to step **204**. If the decoding is successful, the method continues in step **220**.

In step **220**, an acknowledgement is sent to the TS in order for the TS to stop sending the current packet. The method continues in step **222**.

In step **222**, the processing of the current packet stops.

In step **224**, the value of the auxiliary variable k is increased by 1. The method continues in step **226**.

In step **226**, the condition $k > n + m$ is evaluated. If the condition $k > n + m$ is satisfied, the method continues in step **228**. If the condition $k > n + m$ is not satisfied, the method returns to step **214**.

In step **228**, a decoding attempt with currently available data is carried out for a pre-determined number of iterations N_{n+m+1}. Selection of N_{n+m+1} as $N_1 \leq \ldots \leq N_m \geq N_{m+1} \geq N_{m+2} \geq \ldots > N_{n+m+1}$ is reasonable because if the slot actually has a very good SINR, then the slot is very likely to be correctly decoded with a very small number of iterations.

One skilled in the art will understand that the interval testing decision steps (**208**, **214**, and **228**) is shown as being tested sequentially for illustrative purposes only. Other possibilities include parallel interval testing or a combination thereof.

In one embodiment of the invention, a dynamic stopping rule (described below) is used in conjunction with the above-mentioned rules. The dynamic stopping rule prevents the decoder from running too many iterations after the packet has been successfully decoded.

In another embodiment, a decoder carries out a decoding process as a single action. Then, the early termination method is as follows:

If $AS < TS$, do not attempt to decode the current packet with currently available data.

If $AS \geq TS$, attempt to decode the packet.

Turbo Decoding with Dynamic Stopping Rule

In one embodiment of the invention, turbo codes are used for encoding packets for transmission. Turbo codes, known to one of ordinary skill in the art, are described in, e.g., Chris Heegard and Stephen B. Wicker, Turbo Coding (1999), which is incorporated herein by reference. Turbo decoding is an iterative procedure, in which each subsequent iteration increases the level of confidence that the packet has been successfully decoded. Consequently, a significant power saving is achieved by stopping the iterative decoding procedure as soon as the packet has been decoded successfully.

There are several dynamic stopping rules known to one of ordinary skill in the art. One embodiment may utilize cross entropy criteria to determine when to stop the iterative decoding process. Such a criterion is disclosed in "Iterative Decoding of Binary Block Codes," by Joachim Hagenauer, Elke Offer and Lutz Papke, IEEE Trans. Information Theory, Vol. 42, No. 2, pp. 429-445 (March 1996), which is incorporated herein by reference.

In another embodiment of the invention, when the RS **104** decides to attempt packet decoding, the iterative decoding procedure is carried out for at least a minimum number of iterations N_{min}, and at most a maximum number of iterations N_{max}. In one embodiment, N_{min} and N_{max} are determined in accordance with simulations or controlled tests of demodulator performance under various channel conditions. After the first N_{min} iterations, a quality metric of the decoded payload is computed, and compared to a quality metric contained in the decoded packet. In one embodiment, the quality metric is a cyclic redundancy check (CRC). If the two CRCs are equal, then the CRC is said to be valid. If the CRC is valid, decoding for a successive iteration is carried out and a CRC of a decoded payload is computed, and compared to a CRC contained in the decoded packet. If the CRCs computed after two successive iterations are identical and valid, then the decoding is deemed to be successful, and terminated. If the CRCs computed after two successive iterations are not

identical or not valid, decoding for additional m iterations is carried out and the test is repeated. In any case, decoding is terminated after N_{max} iterations. After the first N_{max} iterations, a CRC of the decoded payload is computed, and compared to a CRC contained in the decoded packet. If the two CRCs are equal, then the packet is declared successfully decoded. The above-described method is disclosed in co-pending application serial number 09/350,941 entitled "EFFICIENT ITERATIVE DECODING," filed July 9, 1999, assigned to the assignee of the present invention, and incorporated herein by reference.

Acknowledgement Procedure

As previously mentioned, when the RS **104** successfully decodes the current packet before it has been transmitted in entirety, the RS **104** sends an acknowledgement to the TS **102**. In response, the TS **102** stops sending the current packet.

FIG. 3 illustrates a conceptual forward link structure in accordance with one embodiment of the invention. A multi-slot packet is transmitted from TS **102** (FIG. 1) to RS **104** (FIG. 1) in successive slots. The transmission of the first slot of the starts in the n-th slot. The RS **104** decodes the packet, and verifies the CRC of the decoded result after having received the $(n+1)$th slot of transmission. The RS **104** informs the TS **102** about the outcome by sending a FAST_ACK signal in the slot $(n+4)$. The TS **104** demodulates and interprets the FAST_ACK signal and terminates transmission of the current packet in the slot $(n+4)$. Thus, although the transmission of the current packet has been terminated early, if the scheduling method retransmitted the current packet in the interval between the $(n+1)$th slot and the $(n+5)$th slot, some transmission waste occurred. One skilled in the art will understand that the correspondence between the actions and slots is for illustrative purposes only. Thus, implemented system may take different interval than two slots between decoding a slot and sending a FAST_ACK signal.

FIG. 4 illustrates a conceptual forward link structure in accordance with another embodiment of the invention. The transmission of the first slot of a multi-slot packet from TS **102** (FIG. 1) to RS **104** (FIG. 1) starts in the n-th slot. Each successive slot of the multi-slot packet is transmitted m slots later. The value of m is determined to allow the RS **104** to decode the packet after each additional slot of transmission, verify the CRC of the decoded result, and inform the TS **102** about the outcome, before the RS **104** receives the next slot. If the RS **104** manages to decode the packet before the normal packet transmission is complete, it sends an FAST_ACK signal to the TS **102** before the next slot of the current packet is sent. The TS **102** demodulates and interprets the

FAST_ACK signal sufficiently in advance to terminate transmission of the current packet. The TS **102** may then transmit a new packet to the RS **104** or a different RS, during the period in which it would have otherwise transmitted the original packet.

5   Note that the term "FAST_ACK signal" that is described herein is different from the acknowledge messages that may be sent by the higher layers of automatic request protocols (ARQ) such as RLP, TCP and other protocols known to one of ordinary skill in the art.

FIG. 5 illustrates elements of an apparatus 500 in accordance with one
10   embodiment of the present invention.

The apparatus **500** comprises a processor **502** and a storage medium **504** accessible by the processor **502** and containing a set of instructions readable and executable by the processor **502**. The apparatus **500** further comprises an interface **506** accessible by the processor **502**, allowing the apparatus **500**
15   communicate with other logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein.

Those of skill in the art would understand that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic
20   hardware, computer software, or combinations of both. The various illustrative components, blocks, modules, circuits, and steps have been described generally in terms of their functionality. Whether the functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans recognize the
25   interchangeability of hardware and software under these circumstances, and how best to implement the described functionality for each particular application.

As examples, the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed
30   herein may be implemented or performed with a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components such as, e.g., registers and FIFO, a processor executing a set of firmware instructions, any conventional
35   programmable software module and a processor, or any combination thereof. The processor may advantageously be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. The software module could reside in RAM memory, flash memory, ROM memory, registers, hard disk, a removable disk, a CD-ROM, or

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any other form of storage medium known in the art. Those of skill would further appreciate that the data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description are advantageously represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

1.   A method for reducing power consumption of a decoder in a
2   communication system, comprising:
    estimating a quality metric of a segment of a received signal;
4   determining a quality metric threshold;
    delimiting an interval in accordance with a modified quality metric
6   threshold; and
    decoding the segment when the estimated quality metric is outside of the
8   interval.

2.   The method of claim 1 wherein the estimating a quality metric comprises
2   estimating a signal-to-noise ratio.

3.   The method of claim 1 wherein the estimating a quality metric of a
2   segment of a received signal comprises estimating a quality metric of a slot of a
    received signal.

4.   The method of claim 1 wherein the determining a quality metric
2   threshold comprises:
    determined a data rate of the segment;
4   determining a number of segments received; and
    determining a quality metric threshold in accordance with the data rate
6   and the number of segments.

5.   The method of claim 1 wherein delimiting an interval comprises:
2   determining a real-valued parameter Δ_0; and
    defining the interval in accordance with a formula $(-\infty, TS + \Delta_0)$, where
4   TS is the quality metric threshold.

6.   The method of claim 5 wherein the determining a real-valued parameter
2   Δ_0 comprises determining the parameter Δ_0 in accordance with a demodulator
    performance.

7.   The method of claim 5 wherein the parameter Δ_0 is less than or equal to
2   zero.

8.   The method of claim 1 wherein the decoding the segment comprises:

2   delimiting a plurality of intervals in accordance with the quality metric threshold;

4   associating each of the plurality of intervals with one of a plurality of parameters;

6   determining an interval from the plurality of intervals into which the estimated quality metric belongs; and

8   decoding the received signal for a number of iterations equal to the one of a plurality of parameters associated with the determined interval.

9.   The method of claim 8 wherein the delimiting a plurality of intervals

2   comprises:

4   determining a plurality of real-valued parameters $\Delta_0 \leq \Delta_1 \leq ... \leq \Delta_m \leq 0 < \Delta_{m+1} \leq \Delta_{m+2} \leq ... \leq \Delta_{m+n}$; and

6   defining the plurality of intervals in accordance with the formulas:
$[TS + \Delta_{k-1}, TS + \Delta_k)$, for all $k \in (1, n+m)$; and
$[TS + \Delta_{n+m}, \infty)$,

8   where n, m are non-negative, integer-valued parameters.

10.   The method of claim 9 wherein the parameters

2    $\Delta_1, ..., \Delta_m, \Delta_{m+1}, \Delta_{m+2}, ..., \Delta_{m+n}$ are determined in accordance with a demodulator performance.

11.   The method of claim 8 wherein a plurality of parameters comprise non-

2   negative, integer-valued parameters $N_1 \leq ... \leq N_m \geq N_{m+1} \geq N_{m+2} \geq ... > N_{n+m+1}$.

12.   The method of claim 11 wherein the parameters

2    $N_1, ..., N_m, N_{m+1}, N_{m+2}, ..., N_{n+m+1}$ are determined in accordance with a demodulator performance.

13.   The method of claim 1 further comprising:

2   evaluating a stopping criterion; and
terminating decoding in accordance with the stopping criterion.

14.   An apparatus for reducing power consumption of a decoder in a

2   communication system, comprising:
a processor; and

4   a processor-readable storage medium accessible by the processor and containing a set of instructions executable by the processor to:

6   estimate a quality metric of a segment of a received signal;

determine a quality metric threshold;

8   delimit an interval in accordance with a modified quality metric threshold; and

10   decode the segment when the estimated quality metric is outside of the interval.

15. The apparatus of claim 14 wherein the quality metric is a signal-to-noise

2   ratio.

16. The apparatus of claim 14 wherein the segment of a received signal is a

2   slot.

17. The apparatus of claim 14 wherein the quality metric threshold is

2 determined in accordance with a data rate of the segment and a number of segments received.

18. The apparatus of claim 14 wherein the set of instructions is further

2 executable by the processor to delimit the interval by:

     determining a real-valued parameter Δ_0; and

4   defining the interval in accordance with a formula $(-\infty, TS + \Delta_0)$, where TS is the quality metric threshold.

19. The apparatus of claim 18 wherein the parameter Δ_0 is determined in

2 accordance with a demodulator performance.

20. The apparatus of claim 18 wherein the parameter Δ_0 is less than or equal

2 to zero.

21. The apparatus of claim 14 wherein the set of instructions is further

2 executable by the processor to decode the segment by:

     delimiting a plurality of intervals in accordance with the quality metric

4 threshold;

     associating each of the plurality of intervals with one of a plurality of

6 parameters;

     determining an interval from the plurality of intervals into which the

8 estimated quality metric belongs; and

     decoding the received signal for a number of iterations equal to the one

10 of a plurality of parameters associated with the determined interval.

22. The apparatus of claim 21 wherein the set of instructions is further executable by the processor to delimit a plurality of intervals by:

    determining a plurality of real-valued parameters $\Delta_0 \leq \Delta_1 \leq ... \leq \Delta_m \leq 0 < \Delta_{m+1} \leq \Delta_{m+2} \leq ... \leq \Delta_{m+n}$; and

    defining the plurality of intervals in accordance with the formulas:

$$[TS + \Delta_{k-1}, TS + \Delta_k), \text{ for all } k \in (1, n+m); \text{ and}$$

$$[TS + \Delta_{n+m}, \infty),$$

where n, m are non-negative, integer-valued parameters.

23. The apparatus of claim 22 wherein the parameters $\Delta_1, ..., \Delta_m, \Delta_{m+1}, \Delta_{m+2}, ..., \Delta_{m+n}$ are determined in accordance with a demodulator performance.

24. The apparatus of claim 21 wherein a plurality of parameters comprise non-negative, integer-valued parameters $N_1 \leq ... \leq N_m \geq N_{m+1} \geq N_{m+2} \geq ... > N_{n+m+1}$.

25. The apparatus of claim 24 wherein the parameters $N_1, ..., N_m, N_{m+1}, N_{m+2}, ..., N_{n+m+1}$ are determined in accordance with a demodulator performance.

26. The apparatus of claim 14 wherein the set of instructions further comprises instructions executable by the processor to:

    evaluate a stopping criterion; and

    terminate decoding in accordance with the stopping criterion.

27. A processor-readable medium for reducing power consumption of a decoder in a communication system, comprising instructions executable by processor to:

    estimate a quality metric of a segment of a received signal;

    determine a quality metric threshold;

    delimit an interval in accordance with a modified quality metric threshold; and

    decode the segment when the estimated quality metric is outside of the interval.

28. The processor-readable medium of claim 27 wherein the quality metric is a signal-to-noise ratio.

29.   The processor-readable medium of claim 27 wherein the segment of a

2   received signal is a slot.

30.   The processor-readable medium of claim 27 wherein the quality metric

2   threshold is determined in accordance with a data rate of the segment and a
number of segments received.

31.   The processor-readable medium of claim 27 wherein the set of

2   instructions is further executable by the processor to delimit the interval by:
determining a real-valued parameter Δ_0; and

4   defining the interval in accordance with a formula $(-\infty, TS + \Delta_0)$, where
TS is the quality metric threshold.

32.   The processor-readable medium of claim 31 wherein the parameter Δ_0 is

2   determined in accordance with a demodulator performance.

33.   The processor-readable medium of claim 31 wherein the parameter Δ_0 is

2   less than or equal to zero.

34.   The processor-readable medium of claim 27 wherein the set of

2   instructions is further executable by the processor to decode the segment by:
delimiting a plurality of intervals in accordance with the quality metric

4   threshold;
associating each of the plurality of intervals with one of a plurality of

6   parameters;
determining an interval from the plurality of intervals into which the

8   estimated quality metric belongs; and
decoding the received signal for a number of iterations equal to the one

10 of a plurality of parameters associated with the determined interval.

35.   The processor-readable medium of claim 27 wherein the set of

2   instructions is further executable by the processor to delimit a plurality of
intervals by:

4   determining   a   plurality   of   real-valued   parameters
$\Delta_0 \le \Delta_1 \le ... \le \Delta_m \le 0 < \Delta_{m+1} \le \Delta_{m+2} \le ... \le \Delta_{m+n}$; and

6   defining the plurality of intervals in accordance with the formulas:
$[TS + \Delta_{k-1}, TS + \Delta_k)$, for all $k \in (1, n+m)$; and

8       $[TS + \Delta_{n+m}, \infty)$,

where n, m are non-negative, integer-valued parameters.

36. The processor-readable medium of claim 35 wherein the parameters $\Delta_1, ..., \Delta_m, \Delta_{m+1}, \Delta_{m+2}, ..., \Delta_{m+n}$ are determined in accordance with a demodulator performance.

37. The processor-readable medium of claim 27 wherein a plurality of parameters comprise non-negative, integer-valued parameters $N_1 \leq ... \leq N_m \geq N_{m+1} \geq N_{m+2} \geq ... > N_{n+m+1}$.

38. The processor-readable medium of claim 37 wherein the parameters $N_1, ..., N_m, N_{m+1}, N_{m+2}, ..., N_{n+m+1}$ are determined in accordance with a demodulator performance.

39. The processor-readable medium of claim 27 wherein the set of instructions further comprises instructions executable by the processor to:
    evaluate a stopping criterion; and
    terminate decoding in accordance with the stopping criterion.

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ABSTRACT

A method and an apparatus for reducing power consumption of a decoder in a communication system are disclosed. In a communication system communicating a packet, the packet can be arranged among slots of a communication channel so that each slot following the first slot contains redundant bits of the packet with respect to the first slot. A receiving station estimates quality metric of a received slot, determines a quality metric threshold, and delimits an interval in accordance with the modified quality metric threshold. If the estimated quality metric is outside of the interval, the segment is decoded. The decoding process comprises delimiting a plurality of intervals in accordance with the quality metric threshold, associating each of the plurality of intervals with one of a plurality of parameters, determining an interval from the plurality of intervals into which the estimated quality metric belongs; and decoding the received signal for a number of iterations equal to the one of a plurality of parameters associated with the determined interval. In the course of the decoding process, a stopping criterion is evaluated, and the decoding process is terminated in accordance with the stopping criterion.
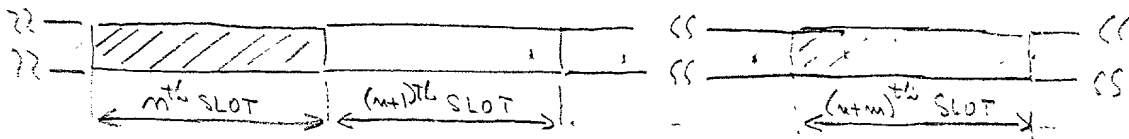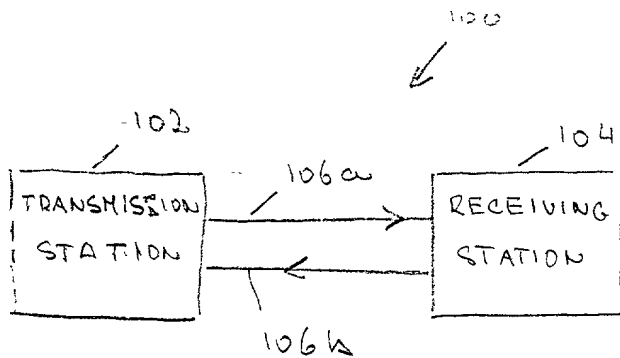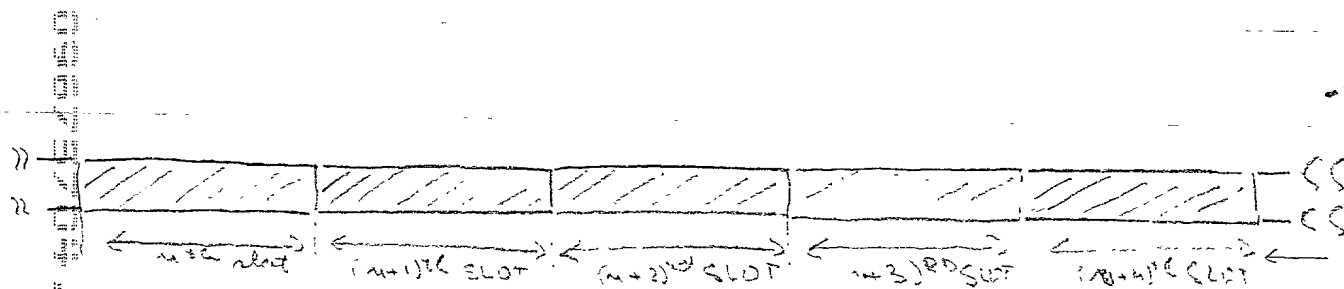
FIG. 4

FIG. 1.

FIG. 3.

PACKET DECODED

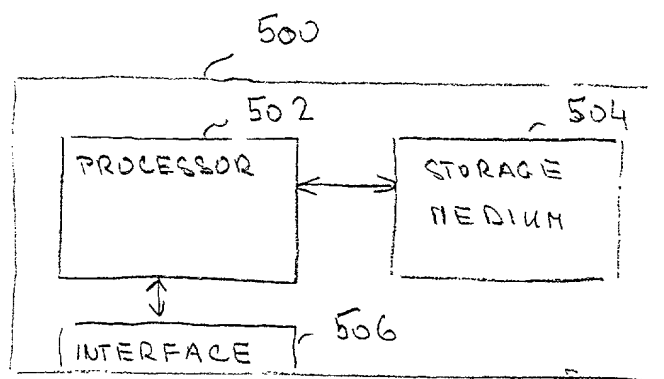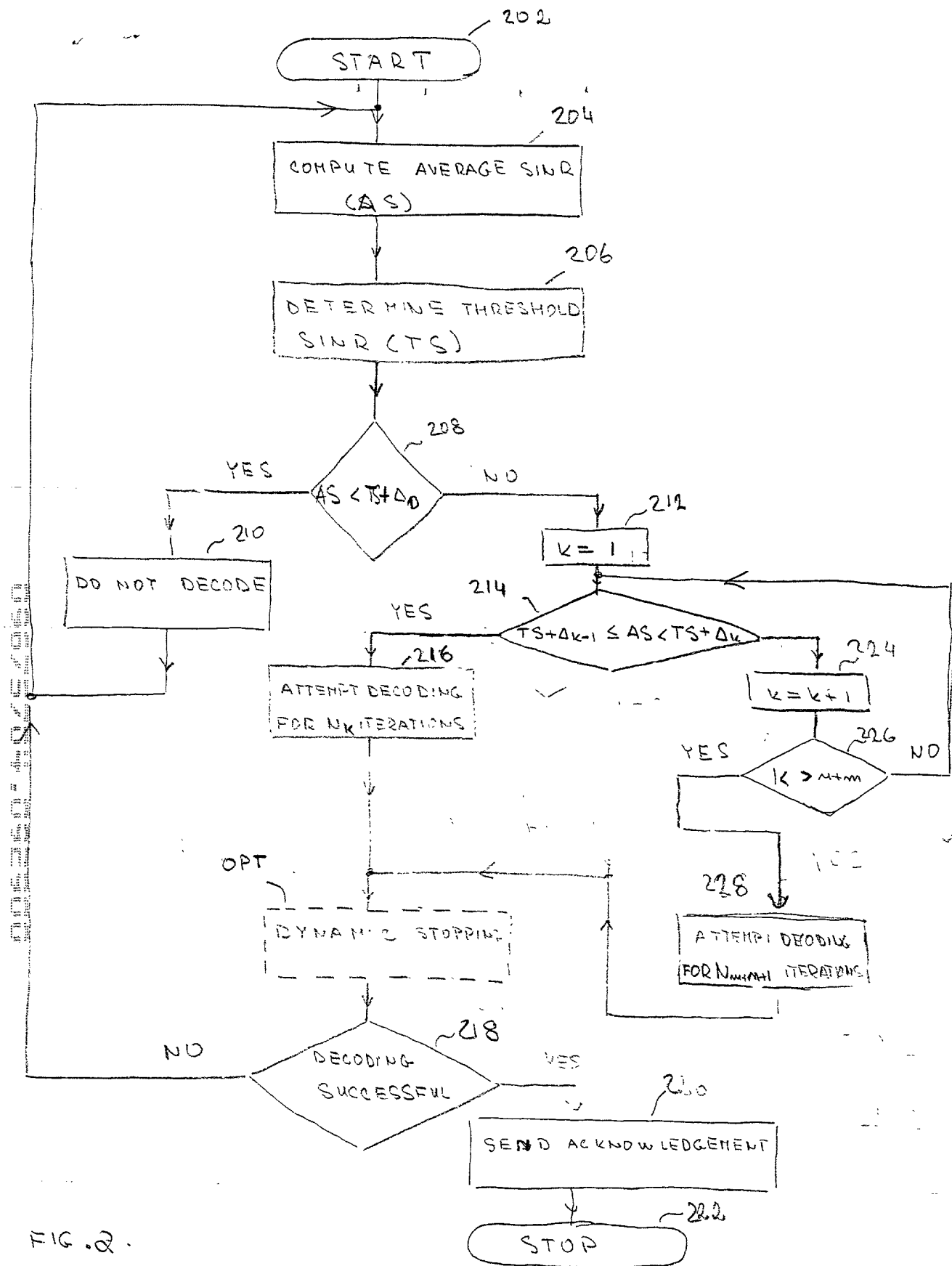ACKNOWLEDGEMENT
SENT

ACKNOWLEDGEMENT
RECEIVED AND
ACTED ON

FIG. 5

START 202

COMPUTE AVERAGE SINR (AS) 204

DETERMINE THRESHOLD SINR (TS) 206

208
$AS < TS + \Delta_0$
YES — NO

DO NOT DECODE 210

$k = 1$ 212

214
$TS + \Delta_{k-1} \leq AS < TS + \Delta_k$
YES — NO

ATTEMPT DECODING FOR N_k ITERATIONS 216

$k = k + 1$ 224

226
$k > M + m$
YES — NO

ATTEMPT DECODING FOR N_{M+M+1} ITERATIONS 228

OPT
DYNAMIC STOPPING

DECODING SUCCESSFUL 218
NO — YES

SEND ACKNOWLEDGEMENT 220

STOP 222

FIG. 2.

COMBINED DECLARATION / POWER OF ATTORNEY

AS BELOW NAMED INVENTOR, I HEREBY DECLARE THAT: This Declaration is of the following type:

☒ Original   ☐ Supplemental   ☐ Continuation-In-Part   ☐ Divisional
☐ Continuation   ☐ National Stage of PCT

My residence, post office address and citizenship are as stated below next to my name: I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION OF A DECODER IN A COMMUNICATION SYSTEM the specification of which:

☒ is attached hereto.
☐ was filed on   as Serial No.   .
☐ was amended on   (if applicable).
☐ was described and claimed in PCT International Application No.   filed on   and as amended under PCT Article 19 on   .

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 of any foreign application(s) for patent or inventor's certificate or of any PCT International application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

			Priority Claimed	
(Country)	(Application No.)	(Day/Month/Year/Filed)	(Yes)	(No)

I hereby claim the benefit under Title 35 USC 120 of the United States application(s) listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 USC 112, I acknowledge the duty to disclose material information as defined in Title 37 CFR 1.56(a) which occurred between the filing date of the prior application and the national or PCT International filing date of this application:

(Serial No.)	(Filing Date)	(Status)

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith: Russell B. Miller, Reg. No. 31,122, Gregory D. Ogrod, Reg. No. 30,880, Bruce W. Greenhaus, Reg. No. 37,339, Charles D. Brown, Reg. No. 28,285, Thomas R. Rouse, Reg. No. 40,793, Kent D. Baker, Reg. No. 38,822, Thomas M. Thibault, Reg. No. 42,181, Tom Streeter, Reg. No. 32,007, Christopher O. Edwards, Reg. No. 36,127, Pavel Kalousek, Reg. No. 44,178, Kyong H. Macek, Reg. No. 42,977, Byron Yafuso, Reg. No. 45,244, Raymond B. Hom, Reg. No. 44,773, Kevin J. Clark, Reg. No. 42,421, Sean English, Reg. No. 37,319, Roger W. Martin, Reg. No. 39,291, Sandip S. Minhas, Reg. No. 44,945, Michael D. Hartogs, Reg. No. 36,547, Philip R. Wadsworth, Reg. No. 29,219, S. Hossain Beladi, Reg. No. 42,311, Albert J. Harnois, Reg. No. 46,123, Sandra L. Godsey, Reg. No. 42,589, and Maryanne E. DeAngelo, Reg. No. P47,288. Please direct all telephone calls to Philip R. Wadsworth at (858) 651-4404 and address all correspondence to: Sarah Kirkpatrick, Manager, Intellectual Property Administration, QUALCOMM Incorporated, 5775 Morehouse Drive, San Diego, California 92121-1714.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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